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# SWITCH MODE POWER SUPPLY CONTROL CIRCUIT

## Field of the Invention

The present invention relates to a system and method for adjusting switching times in a converter such as a buck converter, a boost converter, or a buck-boost converter. A one-shot circuit is configured to dynamically initiate a pulse cycle for the switching converter when the output voltage collapses to a level that is related to a monitored inductor current in the converter.

## Background of the Invention

Buck converters are DC-to-DC converters that are arranged to provide an output voltage that is lower in magnitude than the input voltage. An example buck converter is illustrated in FIGURE 1. The example buck converter includes an oscillator, an on-time control circuit, a driver circuit (DRV), a power switching device (PSW), a diode (D), an inductor (L), a capacitor (C), and a load circuit (LOAD).

The actuating of the power switching device (PSW) coincides with two operating phases. During the first operating phase, the power switching device couples energy from the input voltage source (VIN) to the inductor (L), the capacitor (C), and the load circuit (LOAD). During the second operating phase, the power switching device (PSW) is deactivated and the diode (D) allows the stored energy in the inductor (L) to continue flowing to the capacitor (C) and the load circuit (LOAD). At a later time interval, the oscillator and the on-time control circuit repeat the switching pattern.

## Brief Description of the Drawings

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following drawings.

FIGURE 1 is an illustration of a conventional buck converter.

FIGURE 2 is an illustration of an example embodiment of a buck converter;

FIGURE 3 is an illustration of an example PLL arrangement for a converter;

FIGURES 4A - 4C are illustrations of various waveforms during the operation of a converter; and

FIGURE 5 illustrates an example embodiment of a boost converter, arranged in accordance with at least one aspect of the present invention.

## Detailed Description of the Preferred Embodiment

Various embodiments of the present invention will be described in detail with reference to the drawings, where like reference numerals represent like parts and assemblies throughout the several views. Reference to various embodiments does not limit the scope of the invention, which is limited only by the scope of the claims attached hereto. Additionally, any examples set forth in this specification are not intended to be limiting and merely set forth some of the many possible embodiments for the claimed invention.

Throughout the specification and claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates otherwise. The meanings identified below are not intended to limit the terms, but merely provide illustrative examples for the terms. The meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The term "coupled" means either a direct electrical connection between the items connected or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal.

Briefly stated, the invention is related to an apparatus and method for dynamically adjusting a pulse width (e.g., off-time pulse) associated with a switching device in a converter such as a buck converter, a boost converter, or a buck-boost regulator. A one-shot circuit is configured to dynamically initiate a pulse cycle for the

switching converter when the output voltage collapses to a level that is related to a monitored inductor current in the converter. By changing the start time associated with the one-shot circuit, the pulse-width (e.g., off-time pulse) associated with the switching device is varied. In one example, the one-shot circuit is triggered when the inductor current is sensed as decaying below a threshold. The one-shot circuit can be further arranged to have another pulse-width (e.g., on-time pulse) that is adjusted for phase alignment with a reference frequency using a PLL circuit.

FIGURE 2 is an illustration of an example embodiment of a buck converter that is arranged according to at least one aspect of the present invention. The example buck converter includes an oscillator (OSC), a phase-locked loop (PLL) circuit, a one-shot circuit, a driver circuit (DRV), a switching device (SW), a diode (D), an inductor (L), a capacitor (C), three resistors ($R_{SNS}$, $R_{FB}$, $R_{FF}$), a reference circuit (REF), a feedback circuit (FB), trans-conductance amplifier ($g_m$) circuit, and a comparator circuit (CP).

The switching device (SW) is any appropriate switching device or circuit that is configured to selectively pass energy when activated. In one example, the switching device (SW) is a p-type device such as a metal oxide semiconductor device (MOS) or some other field effect device (FET). In another example, the switching device (SW) is an n-type device such as a metal oxide semiconductor device (MOS) or some other field effect device (FET).

The reference circuit (REF) can be any appropriate reference circuit that is arranged to provide a reference voltage ($V_{REF}$) to resistor $R_{FB}$. In one example, the reference circuit (REF) is a band-gap circuit.

Switching device SW is configured to couple energy to the inductor from the input source ($V_{IN}$) when operated in a closed-circuit position in response to a switch control signal (SWCTL). The diode (D) is arranged to permit current flow from the low supply (e.g., GND) through the inductor via resistor $R_{SNS}$ when the switching device is in an open-circuit position. The output of the one-shot circuit initiates actuation of the switching device via an optional driver circuit (DRV).

The comparator (CP) is arranged to trigger a start signal (START) for the one-shot circuit in response to a comparison between the sensed feedback voltage ($V_{FB}$) from the switching regulator and another voltage ($V_X$) that is related to the current ($I_L$) in the inductor (L) during the open-circuit condition for the switching device (SW).

In one example, the sensed feedback voltage ($V_{FB}$) corresponds to the output voltage ($V_{OUT}$) for the switching regulator. In another example, the sensed feedback voltage ($V_{FB}$) is related to the output voltage ($V_{OUT}$) by a gain scaling factor via a gain circuit (not shown). In still another example, the sensed feedback voltage ($V_{FB}$) is related to the output voltage ($V_{OUT}$) by a divider factor via a voltage divider circuit (e.g., see FIG. 5).

For the example illustrated in FIG. 2, voltage $V_X$ is generated by the cooperation of the trans-conductance amplifier ($g_m$) circuit, resistor $R_{SNS}$, resistor $R_{FB}$, and the reference voltage ($V_{REF}$). Resistor $R_{SNS}$ conducts current ($I_L$) through diode D and inductor L when switching device SW is operated in an open-circuit position. The voltage drop across resistor $R_{SNS}$ is determined by the product $I_L*R_{SNS}$. The $g_m$ circuit converts the sensed voltage into a current ($I_{SNS}$), which is given by: $I_{SNS} = g_m*I_L*R_{SNS}$. Resistor $R_{FB}$ is arranged to cooperate with the reference circuit and a sense current ($I_{SNS}$) to adjust a voltage ($V_X$) based on sensed output voltage from resistor $R_{SNS}$. The reference voltage ($V_{REF}$) provides a nominal value for voltage $V_X$ when the switching device (SW) is operated in a closed-circuit position. The overall value associated with voltage $V_X$ is given by:

$V_X = V_{REF}$, closed-circuit position of SW, and

$V_X = V_{REF} - g_m*I_L*R_{SNS}*R_{FB}$, open-circuit position of SW.

The one-shot circuit can be any appropriate circuit that is arranged to provide a pulse in response to a start signal. In one example, the one-shot circuit is simply an RS-type flip-flop circuit, where the start signal input corresponds to the set input (S). In another example, the one-shot circuit comprises an RS-type flip-flop circuit that is arranged to cooperate with a delay circuit. For this example, the flip-flop is set via the START signal, the delay circuit is initiated via the START signal, and the flip-flop is reset via an output of the delay circuit.

The oscillator circuit (OSC), the phase-locked loop (PLL) circuit, and resistor $R_{FF}$ are optional circuits that can be used to adjust the pulse width associated with the one-shot circuit. The oscillator circuit (OSC) is arranged to provide a reference frequency ($f_{REF}$) to the PLL circuit. Another input of the PLL circuit is responsive to a feedback frequency signal ($f_{FB}$) that is provided by the output of the one-shot circuit. The output of the PLL circuit corresponds to a current ($I_{PLL}$) that is coupled to a biasing input of the one-shot circuit. Resistor $R_{FF}$ is coupled between the biasing input of the one-shot circuit and the input source ($V_{IN}$), such that the biasing current ($I_{BIAS}$) that is provided to the one-shot circuit is responsive to changes in the PLL output current and the input source ($V_{IN}$). The one-shot circuit has a programmable on-time that is responsive to the biasing current ($I_{BIAS}$).

In the buck regulator circuit illustrated in FIGURE 2, the inductor (L) and the capacitor (C) are selected to provide sufficient energy storage to minimize the AC ripple in the output voltage. For example, the inductor value (L) can be selected based upon a desired ramp rate of current ($di/dt = \Delta V/L$). The combination of values for the inductor and the capacitor results in the formation of a system pole in the closed loop operation of the converter.

FIGURE 3 is an illustration of an example PLL arrangement (300) for a converter that is arranged in accordance with at least one aspect of the present invention. The example PLL includes a phase detector, a charge pump, a first capacitor, a filter network, a trans-conductance ($g_m$) circuit, and a current source. An optional bias circuit (BIAS) can be arranged to bias the current source with a biasing signal ($BIAS_{IFF}$) that is responsive to changes in the input voltage ($V_{IN}$). In another example, the current source function can be provided within the trans-conductance ($g_m$) circuit. The current source in FIGURE 3 serves a similar purpose to resistor $R_{FF}$ from FIGURE 2.

The phase detector compares the input frequency $f_{FB}$ from the one-shot circuit to the reference frequency ($f_{REF}$). The output of the phase detector is a pair of selection signals for selecting increasing and decreasing currents from the charge pump. The charge pump generates voltage $V_{BIAS}$ from by coupling the increasing and decreasing currents to the filter network. Voltage $V_{BIAS}$ is converted to a current ($I_{PLL}$)

via the trans-conductance ($g_m$) circuit. The current source provides a current ($I_{FF}$) that is combined with current $I_{PLL}$ to provide a biasing current ($I_{BIAS}$) to the one-shot circuit.

The pulse-width associated with the one-shot circuit is responsive to the biasing current ($I_{BIAS}$). In one example, the pulse-width associated with the one-shot is related to a charge time associated with a capacitor, where the charge time is adjusted by changing the biasing current ($I_{BIAS}$). The PLL circuit is arranged to adjust the on-time associated with the switching device (or circuit) by adjusting the pulse-width associated with the one-shot circuit. The PLL circuit adjusts the pulse-width of the one-shot circuit so that the frequency ($f_{FB}$) of the one-shot circuit is phase aligned with the reference frequency ($f_{REF}$).

Although the above described PLL circuit required frequency compensation for proper operation, the frequency compensation is not dependent on the values associated with the inductor (L) and the capacitor (C). Since the inductor and capacitor can be selected independent of the PLL compensation, users of an integrated circuit implementation have increased power supply design flexibility. The frequency compensation of the PLL circuit is analyzed as follows below.

The one-shot circuit is arranged to generate a pulse that has a variable pulse-width ($t_{ON}$). The pulse-width ($t_{ON}$) is responsive to variations in a biasing current ($I_{BIAS}$), which is determined in part by a control voltage ($V_{BIAS}$). The frequency ($f_{FB}$) of the pulses from the one-shot circuit are related to the pulse-width ($t_{ON}$). For stable closed loop operation, changes in frequency $\Delta f_{FB}$ are directly related to changes in the biasing voltage ($\Delta V_{BIAS}$) as a constant ($K_{VCO}$). In other words, $K_{VCO} = \Delta f_{FB}/\Delta V_{BIAS}$.

For a buck converter, the duty cycle of the converter circuit is given as: duty cycle = $V_{OUT}/V_{IN} = t_{ON}*f_{FB}$. As described previously, the one-shot circuit has a delay that can be implemented (or modeled) as a current ($I_{OS}$) that is fed into a capacitor ($C_{OS}$) to generate a voltage ramp. Current $I_{OS}$ has a level that is set by $I_{BIAS}$. The rate of the voltage ramp ($\Delta V/\Delta t$) on the capacitor ($C_{OS}$) is determined by the level of current $I_{OS}$ and the value of capacitor $C_{OS}$. Changes in the on-time interval ($\Delta t_{ON}$) for the converter corresponds are determined as: $\Delta t_{ON} = \Delta V_{OS}*C_{OS}/I_{BIAS} = \Delta V_{OS}*C_{OS} / I_{PLL}$, where: $I_{PLL} = V_{BIAS}*gm_{PLL}$, $\Delta V_{OS}$ corresponds to the change in voltage on capacitor

$C_{OS}$, and $gm_{PLL}$ corresponds to the trans-conductance associated with the buffer in the PLL circuit.

The frequency from the output of the one-shot circuit ($f_{FB}$) is related to the on-time interval ($t_{ON}$) as: $f_{FB} = V_{OUT}/(V_{IN}*t_{ON})$. The ratio of the frequency of output pulses from the one shot circuit ($f_{FB}$) to the control voltage ($V_{BIAS}$) in the PLL is given by: $f_{FB} / V_{BIAS} = (V_{OUT} / (V_{IN}*t_{ON})) / V_{BIAS}$ , which can be simplified to: $f_{FB} / V_{BIAS} = (V_{OUT} * gm_{PLL}) / (V_{IN}*\Delta V_{OS}*C_{OS})$. In one example, $V_{OUT} = K*V_{REF}$ and $\Delta V_{OS} = m*V_{REF}$, where K is constant that is related to the feedback circuit and m is another constant. For this example, $K_{VCO} = K*gm_{PLL}/(V_{IN}*m*C_{OS})$. It is noteworthy that $K_{VCO}$ is independent of: the output voltage of the converter ($V_{OUT}$), the reference voltage ($V_{REF}$), and $\Delta V_{OS}$, such that the stability of the PLL is an independent parameter relative to the converter.

In another example, an optional bias circuit can be arranged to provide dynamic $g_m$ of the trans-conductance circuit in the PLL. For this example, $gm_{PLL} = k*V_{IN}$ and $K_{VCO}$ is simplified further to: $K_{VCO} = K*k* gm_{PLL} / (m*C_{OS})$. A similar arrangement can be provided via the current source illustrated in the PLL circuit shown in FIG. 3.

FIGURES 4A - 4C are illustrations of various waveforms during the operation of a converter that is arranged in accordance with at least one aspect of the present invention. For each of the figures, the switching device (or circuit) is in: a closed-circuit operating condition during an on-time interval ($t_{ON}$), and an open-circuit operating condition during an off-time interval ($t_{OFF}$).

In FIG. 4A, the load condition is relatively constant such that the output voltage ($V_{OUT}$) various over a limited range such as a ripple in the voltage. A first on-time interval is initiated at point $P_1$ for a defined pulse width. During the on-time interval ($t_{ON}$), energy is stored in the inductor of the switching regulator such that the output voltage increases, and voltage $V_X$ corresponds to $V_{REF}$. After the on-time interval expires, the off-time interval commences for a variable time duration ($t_{OFF}$). During the off-time interval the output voltage ($V_{OUT}$) decreases. The off-time interval ($t_{OFF}$) is terminated when the sensed inductor current ($I_L$) decays sufficiently that

voltage $V_X$ intersects the output voltage ($V_{OUT}$) as illustrated by point $P_2$. Voltage VX appears as a chopped saw-tooth waveform as illustrated in the figure.

In FIG. 4B, the current demanded from the load increases from a first load condition ($I_{LOAD1}$) to a second load condition ($I_{LOAD2}$). During the first load condition ($I_{LOAD1}$), the output voltage has a nominal value corresponding to $V_{OUT1}$ and the pulse width associated with the off-time interval ($t_{OFF1}$) remains relatively constant. At point $P_3$, the load condition begins to change and output voltage ($V_{OUT}$) begins to decrease. At the next off-time interval ($t_{OFF2}$), the off time is shortened relative to the preceding off-time interval ($t_{OFF1}$) since voltage $V_X$ intersects the output voltage in a shortened time period as illustrated by point $P_4$. After the load transition stabilizes, the output voltage settles to a new nominal value corresponding to $V_{OUT2}$ and the pulse-width of the off-time interval becomes relatively constant. The effect is an instantaneous increase in duty cycle, which allows an increase in current that is rapidly delivered to the output.

In FIG. 4C, the current demanded from the load decreases from a first load condition ($I_{LOAD1}$) to a second load condition ($I_{LOAD2}$). During the first load condition ($I_{LOAD1}$), the output voltage has a nominal value corresponding to $V_{OUT1}$ and the pulse width associated with the off-time interval ($t_{OFF1}$) remains relatively constant. At point $P_3$, the load condition begins to change and output voltage ($V_{OUT}$) begins to increase. At the next off-time interval ($t_{OFF2}$), the pulse-width is extended relative to the preceding time off-time interval ($t_{OFF1}$) since voltage $V_X$ intersects the output voltage in an extended time period as illustrated by point $P_4$. After the load transition stabilizes, the output voltage settles to a new nominal value corresponding to $V_{OUT2}$ and the pulse-width of the off-time interval becomes relatively constant.

As illustrated by FIG. 4B, the output voltage decreases when the load demands more current (increased load condition). As illustrated by FIG. 4C, the output voltage increases when the load decreases its current demand (decreased load condition). The net effect of FIGS, 4A-4C is that the output voltage (VOUT) is related to the load condition with a measurable load-line characteristic. By adjusting the scaling factors (e.g., $g_m$, $R_{SNS}$, $R_{FB}$, $V_{REF}$, etc.) a defined range for load-lines can be

provided. Although the output voltage has shifted due to the change in the load condition, the ripple factor is maintained at a minimum level.

FIGURE 5 illustrates an example embodiment of a boost converter that is arranged in accordance with at least one aspect of the present invention. The example boost converter includes a phase-locked loop (PLL) circuit, a one-shot circuit, a driver circuit (DRV), a switching device (SW), a diode (D), an inductor (L), a capacitor (C), three resistors ($R_{SNS}$, $R_{FB}$, $R_{FF}$), a feedback circuit (FB), a trans-conductance amplifier ($g_m$) circuit, a comparator circuit (CP), and a load circuit ($Z_L$).

The example switching device (SW) illustrated in FIG. 5 is an n-type transistor. The switching device (SW) is coupled between the inductor and resistor RSNS such that the inductor is charged by approximately the full supply voltage when the switching device is activated in response to a switch control signal (SWCTL). The diode (D) is arranged to permit current to flow from the input source (VIN) through the inductor to the capacitor (C), the load circuit ($Z_L$), and the feedback circuit (FB). The output of the one-shot circuit initiates actuation of the switching device via an optional driver circuit (DRV).

The comparator (CP) is arranged to trigger a start signal (START) for the one-shot circuit in response to a comparison between the sensed feedback voltage ($V_{FB}$) from the switching regulator and another voltage ($V_X$) that is related to the current ($I_L$) in the inductor (L) during the closed-circuit condition for the switching device (SW). In FIG. 5, the sensed feedback voltage ($V_{FB}$) is related to the output voltage ($V_{OUT}$) by a divider factor via a voltage divider circuit that is illustrated as two resistors. Other voltage divider circuits can be employed including, an active voltage divider, two or more stacked diodes, a capacitive divider, or some other combination of circuits arranged to provide a divider function.

The operation of the trans-conductance amplifier ($g_m$) circuit, the comparator circuit, and the one-shot circuit is substantially similar to that previously described. However, the one-shot circuit is triggered during the on-time of the switching device (or circuit) such that the output voltage ($V_{OUT}$) is boosted relative to the input supply ($V_{IN}$).

The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.